IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Karl M.J. Lofgren et al.		
Assignees:	SanDisk Corporation and Western Digital Corporation		
Title:	Device and Method for Controlling Solid-State Memory System		
Application No.:	10/785,373	Filing Date:	February 23, 2004
Examiner:	Mai, Son Luu	Group Art Unit:	2827
Docket No.:	SNDK.015US6	Conf. No.:	8958

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APPELLANT'S BRIEF UNDER 37 C.F.R. 41.37

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Pursuant to 37 C.F.R. § 1.191 and the Notice of Appeal filed in this application on April 26, 2006, Applicants submit this Appeal Brief. An accompanying petition requests a three-month extension of time, extending the time allowed for filing this appeal brief to September 26, 2006. In accordance with 37 C.F.R. § 41.20(b)(2), the fee of $500.00 for this Appeal Brief has been authorized via EFS. The Commissioner is also authorized to deduct any other amounts required for this Appeal Brief and to credit any amounts overpaid to Deposit Account No. 502664.

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I. REAL PARTY IN INTEREST

The real parties in interest are SanDisk Corporation, a corporation of the state of Delaware, and Western Digital Corporation, a corporation of the state of Delaware, the assignees of all rights, titles and interests in the present patent application from the inventors, Karl M. J. Lofgren, Robert D. Norman, Jeffrey Donald Stai, Anil Gupta and Sanjay Mehrotra.

II. RELATED APPEALS AND INTERFERENCES

A Notice of Appeal was filed on May 3, 2006, for US patent application number 10/809,061, which is a continuation of the present application.

III. STATUS OF THE CLAIMS

The subject application was filed February 23, 2004, and is a continuation of Application No. 09/939,290, filed on August 22, 2001, which is a continuation of Application No. 09/657,369, filed on September 8, 2000, now Patent No. 6,317,812, which in turn is a continuation of Application No. 09/064,528, filed on April 21, 1998, now Patent No. 6,148,363, which in turn is a continuation of Application No. 08/931,193, filed on September 16, 1997, now Patent No. 5,806,070, which in turn is a continuation of Application No. 08/396,488, filed on March 2, 1995, now abandoned, which in turn is a divisional of Application 1 No. 07/736,733, filed on July 26, 1991, now Patent No. 5,430,859. The original parent application claims 1-39 were cancelled in a Preliminary Amendment filed concurrently with the subject application on February 23, 2004. This Preliminary Amendment also added claims 40-54, which were respectively exact copies of claims 1-15 of U.S. patent number 6,525,986, of Prutchi *et al.* issued February 25, 2003.

An Office Communication mailed on August 17, 2004, was a 30-day, non-extendable requirement for information under 37 CFR 1.607 based upon the pending claims having been filed, to which a response was filed on September 16, 2004. An Office Action mailed on July 1, 2005, rejected the claims under the written description requirement of 35 U.S.C. §112, first paragraph, and under 35 U.S.C. §135(b), to which a reply was filed on September 28, 2005. An Office Action mailed on December 29, 2005, again rejected the pending claims under the written description requirement of 35 U.S.C. §112, first paragraph, and made the rejection final.

Claims 1-39 have been cancelled and claims 40-54 are unchanged from the form in which they were originally added. Claims 40-54 stand rejected under 35 U.S.C. §112, first paragraph, as the Applicants allegedly failed to comply with the written description requirement with respect to the element of "a portion of the received address" and similar such language.

IV. STATUS OF AMENDMENTS

On April 26, 2006, a Notice of Appeal from the Examiner's decision rejecting claims 40-54 was filed. No Amendments have been filed since the December 29, 2005, mailing date of the Office Action from which this Appeal is being taken.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As background, this section gives a summary of the present invention. Since the claims stand rejected under the written description requirement of 35 U.S.C. §112, first paragraph, some of this material is presented in more detail below in section VII in order to demonstrate that the specification of the subject application fulfils the written description requirement.

The claimed subject matter relates to methods of addressing memory chips in a memory system having multiple chips. Specifically, the claims present a first and second memory chip, where each of these chips has a different corresponding settable code or key. When an address is received, a portion of it is then compared with these codes with one of the chips enabled, and the other chip disabled, based upon the comparisons.

Such an arrangement of memory chips is shown in the present application in Figures 2A and 2B. Each of the memory chips 141 have a set of pins 147 that are attached to the pads of a mount 149. The pads are selective grounded, as at 161, to set a key or code in each chip to designate a chip address in the array. In Figure 2A, all five pins 147 are used to distinguish between the chips of a multi-chip module. In Figure 2B, two of the pins 147 are used to supply the code or key distinguishing the chips of a given submodule, the other pins being used to distinguish the different submodules. Figure 2A is described in more detail in paragraphs [0046]-[0050], with Figure 2B described in [0051]-[0053]. (The references are to the clean version of the Substitute Specification included when the present application was filed.)

Figure 4 shows an example of a memory chip 141 including device select circuit 203, which is shown in more detail in Figures 5A and 5B that is described beginning at paragraph [0062]. The embodiment of Figure 5A is primarily described beginning at paragraph [0067] and the timing diagram 5B is described in paragraph [0071]. As shown in Figures 2A and 2B, device bus 135 is connected to all of the memory chips. When an address is received at chip in shift register 311 (Figure 5A), it is then provided to the comparator 305 to compare with the key or code set on pins 147. Based upon this comparison, a chip is selected when the code is matched and not selected if the code is not matched, as described in paragraph [0069].

For example, a read operation is described in paragraph [0091]. The entire address of the memory "chunk" (the unit in which data is read and written in the application) consists of the chip address followed by the address of a "chunk" on the chip. As described at paragraph [0071], when received at the chip, six bits of this entire chip-plus-chunk address, including the five-bit chip address are loaded into shift register 311. Of these six bits, five are then transferred to Comparator 305 to compare against the pattern set by pad 149 on pins 147 in order to determine whether the chip is enabled or not. (In the arrangement of Figure 2A, all five pins 147 are used to differentiate the chips, while in Figure 2B two pins differentiate between chips on a given submodule, the other pins differentiating between submodules.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Board is asked to review the correctness of the rejections under 35 U.S.C. §112, first paragraph. Specifically, claims 40-54 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written requirement with respect to the "comparison of a portion of the received address" elements of the claims.

More specifically, the Office Action states:

> As to claims 40, 45 and 51, the specification, as originally filed, lacks support for the following recitations: "enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code" (claim 40); "receiving a portion of an address at the first memory chip and at the second memory chip; comparing the portion of the address to the first selection code and to the second selection code" (claim 45), and "receiving a portion of an address at the first memory chip; enabling the first memory chip if the received address portion matches the first code" (claim 51). Nowhere in the specification

> mentions about comparing a portion of a received address with a programmable code.

The emphasis is in the Office Action. Claims 41-44, 46-50, and 52-54 are rejected as they respectively depend on claims 40, 45, and 51. This is the basis for rejecting all of the claims and is the sole issues in this appeal.

All of the claims stand rejected under the same grounds and can be taken to form a single group, with independent claim 40 suitable for deciding whether this group of claims patentable.

VII. ARGUMENT

The most recent Office Action, from which this Appeal originates, rejects all of the pending claims under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement for the "comparison of a portion of the received address" element, as described in the preceding section. All of the claims are rejected on the same grounds, with all of the claims are argued together and, when reference to a specific claim is required, claim 40 is believed suitable for this purpose. As described below, it is believed that the written description is fully met.

First, however, it should be noted that it appears that the Office Action is requiring not just support for the claims as written, for a *specific embodiment that is **not** found in the claims.* This is improper. As noted above in Section III above, the currently pending claims in the present application are copies of claims 1-15 of U.S. patent number 6,525,986 of Prutchi *et al.* In the Office Action, subsequent the portion of the rejection cited above, the Office Action continues on to cite a portion of the present application (paragraph [0069], lines 1-8) and then states:

> On the contrary, Pruchi et al. (U.S. Patent 6,525,986) discloses in figure 3 and related text at column 6, a portion of a received address is defined as two most significant bits A15 and A16 of bus 72.

That is, the Office Action is requiring not just that the present application provide an adequate description of the pending claims as written, but is additionally and improperly requiring that the present application provide support for a specific embodiment of the Prutchi patent.

Therefore, the Office Action is requiring that the present application provide not just support for the claims as written, but for a specific embodiment of U.S. patent 6,525,986 of

Prutchi *et al.* This is again improper and the correct question is whether the present specification satisfies the written description requirement for the claims ***as written***.

The present application provides the this written description. Referring to claim 40, the relevant element reads:

> enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code;

where the emphasis is added (and is the same portion emphasized in the Office Action) to indicate the language for which the Office Action finds no written description. It is respectfully submitted that the present application more than meets the written description requirement for the claim *as written*; in fact, it is believed that the application meets this requirement on several bases. (In the following, the references are again to the clean version of the substitute specification that was submitted at the time of filing the present application.)

The addressing of the memory chips by the controller is discussed in the "Controller Module" section that begins on page 18 with paragraph [0082]. The example of a read command in given in paragraph [0091]:

> ... The microprocessor then loads this address into the address control registers 533. The microprocessor then loads the sequencer 543 with the starting address of the read sequence. The sequence starts executing code at *this address*. The sequencer 543 first shifts out the *selected address for selecting a particular memory device chip* 141, *followed by an address of a memory chunk* (e.g. 64 bits) address from the address control registers ...[emphasis added]

Thus, a full address for a "chunk" is a part specifying the memory chip followed by a part specifying the particular "chunk" on the specified chip. (A "chunk" is the unit in which data is written or read in the exemplary embodiment–see, for example, the beginning of paragraph [0093].) Thus, the address received at the memory chips has a first portion used to select a particular memory chip, followed by the portion of the address for a location on the selected chip. It is this first portion of the address that is then compared to the key or code set on a given chip that is then used to determine whether that chip is enabled or not, as discussed above in section III and described in the application at paragraphs [0064]-[0069]. Consequently, the present application does describe the "comparison of a portion of the received address", namely the "address for selecting a particular memory device chip", for enabling a given memory chip.

Further, in addition to the basis given in the preceding paragraph, the written description requirement for the "comparison of a portion of the received address" language of the claim is met on other bases: For example, paragraph [0071] describes Figure 5B, which is a timing diagram for the operation of Figure 5A, that is in turn described in paragraphs [0067]-[0070]. As described there, the address is transferred in two bits at a time in a serial fashion on lines SI0 and SI1. As described in paragraph [0071], the address is clocked into shift register 301, then:

> After three P/D* clock periods, 6 bits have been loaded into the shift register 301 and only the least significant 5 bits are used by the comparator 303.

The comparator 303 is then used to for the comparison of these 5 (of 6) bits to the code or key set for a given chip. Consequently, based on this portion of the specification, the present application also describe the "comparison of a portion of the received address", or, more specifically, a portion of a portion (the 5 bit portion of a 6 bit portion) of the full chip plus chunk address, for enabling a given memory chip.

Yet another basis, in addition to those given in the preceding two paragraphs, for the written description requirement for the "comparison of a portion of the received address" language of the claim is further found in the embodiment of Figure 2B. As shown in Figure 2B, memory chips (141), such as devices #1.1.1-#1.1.4, on a given submodule (here Submodule #1 181) are distinguished by only two bits of the code set by pad 149 on pins 147. Figure 2B is described primarily at paragraphs [0051]-[0053]. As noted in paragraph [0052]:

> For example, with four memory devices 141 per submodule, only two bits of the multi-pin mount 149 need be configured to provide unique addresses on each submodule.

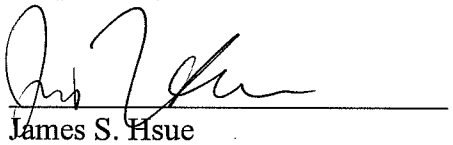
Thus only a portion (two bits) of the five bit chip address will determine whether a given memory chip is enabled or not. Consequently, based on this portion of the specification, the present application also describe the "comparison of a portion of the received address", or, more specifically, a portion (2 bits of the 5 bits) of a portion (the 5 bit portion of a 6 bit portion) of a portion of the full chip plus chunk address, for enabling a given memory chip.

VIII. CONCLUSION

It is Applicants' position, as indicated above, that the assertions of the Office Action are incorrect. As described above, it is believed that disclosure provided by the subject application meets the written description requirement several times over. Accordingly, the rejection of the application should be reversed and the present patent application found allowable.

FILED VIA EFS

Respectfully submitted,



September 25, 2006

James S. Hsue
Reg. No. 29,545

Date

PARSONS HSUE & DE RUNTZ LLP
595 Market Street, Suite 1900
San Francisco, CA 94105
(415) 318-1160 (main)
(415) 318-1162 (direct)
(415) 693-0194 (fax)

Appendix A

CLAIMS PENDING IN APPLICATION SERIAL NO. 10/785,373

(Claims 1-39 have been cancelled.)

40. A method comprising:

receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;

enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and

disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.

41. The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing two or more bits of the received address with the first programmable code.

42. The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing the portion of the received address with a selection logic circuit.

43. The method of claim 40 including comparing the portion of the received address with a first selection logic circuit of the first memory chip and with a second selection logic circuit of the second memory chip.

44. The method of claim 40 further comprising providing the address to a memory array of each of the plurality of memory chips.

45. A method comprising:

assigning a first selection code to a first memory chip and a second selection code to a second memory chip, wherein the second selection code differs from the first selection code;

receiving a portion of an address at the first memory chip and at the second memory chip;

comparing the portion of the address to the first selection code and to the second selection code; and

enabling the first memory chip and disabling the second memory chip based on the comparison.

46. The method of claim 45 further comprising receiving the address at a first memory array of the first memory chip and at a second memory array of the second memory chip.

47. The method of claim 45 wherein assigning includes coupling a bonding pad to a voltage level.

48. The method of claim 45 wherein assigning includes setting a programmable link.

49. The method of claim 45 wherein enabling the first memory chip and disabling the second memory chip based on the comparison includes enabling the first memory chip when the first selection code matches the portion of the address and disabling the second memory chip when the second selection code differs from the portion of the address.

50. The method of claim 45 wherein assigning the first selection code to the first memory chip and the second selection code to the second memory chip includes assigning the first selection code to the first memory chip and separately assigning the second selection code to the second memory chip.

51. A method comprising:

coupling a plurality of address lines of a first memory chip in parallel with a plurality of address lines of a second memory chip;

setting a first code at the first memory chip;

receiving a portion of an address at the first memory chip;

enabling the first memory chip if the received address portion matches the first code; and otherwise disabling the first memory chip.

52. The method of claim 51 wherein enabling the first memory chip includes disabling the second memory chip.

53. The method of claim 51 further including coupling a plurality of data lines of the first memory chip in parallel with a plurality of data lines of the second memory chip.

54. The method of claim 51 further comprising setting a second code at the second memory chip independent of the first code.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.